REMARKS

Claims 1-36 are pending in this application. Claims 1-2, 4-8, 18-19, 21, 30, 33-34, and 36 have been amended to correct informalities. The specification has been amended to correct informalities. No new matter has been added.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the examiner is requested to telephone the undersigned.

It is believed that no fees are due in connection with the filing of this Preliminary Amendment. However, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to the enclosed materials, the Commissioner is hereby authorized to charge any fees to the deposit account No. 19-2386.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on 5/28/02.

Attorney for Applicant(s) — Date of Signature 5/28/02

Respectfully submitted,

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ATTACHMENT A
Version With Markings To Show Changes Made To The Claims

The following is a marked-up version of the amended claims illustrating the newly introduced changes to the claims, in accordance with 37 C.F.R. § 1.121(c)(1)(ii) and (c)(3), showing the changes that the accompanying submission makes to the claims of Application Serial No. 09/916,764. Deleted material is denoted by bold, bracketed type. Added material is denoted by bold, underlined type.

1. (Amended) A computer system comprising:

a **first** processor;

[an interface cable] **a transmission line** coupled to the **first** processor;

a monitor including a receiver input gate coupled to the **[interface cable]** **transmission line**; and

changing circuitry

coupled to the **[interface cable]** **transmission line** and to **[a]** **the** receiver input gate and

capable of changing at least one of a pedestal voltage level on the **[interface cable]** **transmission line** and a signal threshold voltage level of the receiver input gate, such that the pedestal voltage level and the signal threshold voltage level are not substantially equal after the change is made.

2. (Amended) The computer system of claim 1, wherein:

a software program coupled to a **second** processor enables a user of the computer system to initiate the changing at least one of the pedestal voltage level and the signal threshold voltage level.

4. (Amended) The computer system of claim 1, further comprising:
a synchronization processor coupled to the receiver input gate; and
monitoring circuitry
coupled to the synchronization processor and
capable of
monitoring an output of [a] the synchronization processor and
detecting irregularly timed synchronization processor output signals; and
wherein the changing circuitry is further capable of changing at least one of the pedestal voltage level and the signal threshold voltage level when the monitoring circuitry detects irregularly timed output signals.

5. (Amended) The computer system of claim 4, wherein:
the changing is initiated by a software program coupled to a third processor.

6. (Amended) The computer system of claim 4, wherein:
the detecting includes comparing output of [a] the synchronization processor to a stable time reference.

7. (Amended) The computer system of claim 4, wherein:
the detecting includes comparing output of [a] the synchronization processor to phasing of an output of a video amplifier.

8. (Amended) The computer system of claim 1, wherein:
the [interface cable] transmission line carries horizontal synchronization signals.

18. (Amended) The method of claim 17, further comprising:
detecting [am] the effect of signal distortion from reflection on [a] the transmission line caused by a substantial equality of [a] the pedestal voltage level and [a] the signal threshold voltage level.

19. (Amended) The method of claim 17, wherein:

the changing includes using a software program coupled to a **first** processor to initiate the changing.

21. (Amended) The method of claim 17 wherein:

the transmission line is contained in an interface cable connecting

a **[computer] second** processor coupled to a memory; and

the **second** processor **[containing] contains** the signal threshold voltage level.

30. (Amended) The method of claim 29, wherein:

the signal threshold voltage level is changed by changing a reference voltage of the receiver input gate at **[a monitor] an** end of the transmission line **that is coupled to a monitor**.

33. (Amended) The method of claim 31, wherein:

the detecting includes monitoring an output of **[a] the** synchronization processor for irregularly timed output signals by comparison to a stable time reference.

34. (Amended) The method of claim 31, wherein:

the detecting includes monitoring an output of **[a] the** synchronization processor for irregularly timed output signals by comparison to phasing of an output of a video amplifier.

36. (Amended) The method of claim 35, further comprising:

means for detecting **[an] the** effect of signal distortion from reflection on **[a] the** transmission line caused by a substantial equality of **[a] the** pedestal voltage level and **[a] the** signal threshold voltage level.

ATTACHMENT B
Version With Markings To Show Changes Made To The Specification

The following is a marked-up version of the replacement paragraphs illustrating the newly introduced changes to the specification, in accordance with 37 C.F.R. § 1.121(b)(1)(iii), showing the changes that the accompanying submission makes to the specification of Application Serial No. 09/916,764. Deleted material is denoted by bold, bracketed type. Added material is denoted by bold, underlined type.

The paragraph at page 2, lines 4-12, is amended as follows:

Most personal computer systems based on the INTERNATIONAL BUSINESS MACHINES ("IBM®") architecture use an interface cable to connect the monitor to the remainder of the personal computer system. This cable **[ganerally]** **generally** has a characteristic impedance of approximately 30 to 120 Ω and is terminated with an impedance of value Z_t that can range from approximately 2.2 kΩ to 4.7 kΩ or more. This termination impedance is so far removed from the characteristic impedance of the cable that the cable is effectively unterminated. This condition gives rise to reflections of fast signals on the line, which in turn give rise to distortions of those signals. In particular, horizontal synchronization ("h-sync") are sometimes distorted in this way.

The paragraph at page 4, line 25, through page 5, line 11, is amended as follows:

Figure 1 is a block diagram of example computer system 100 that may be found in many forms, including, e.g., mainframes, minicomputers, workstations, servers, personal computers, internet terminals, notebooks, and embedded systems. Personal computer ("PC") systems, such as those compatible with the x86 configuration, include desktop, floor standing, or portable versions. Example computer system 100 includes a computer system hardware unit that further includes a microprocessor (or simply "processor") 110, associated main memory 150, **[and]** a number of peripheral devices that provide I/O for computer system 100, and computer system software that runs on the hardware unit. Example computer system 100 is powered by power

supply 114 with voltage regulator 115. The peripheral devices often include keyboard 191, mouse-type input device 192, CD drive 164, and others not shown, including floppy and hard disk drives, modems, printers, terminal devices, televisions, sound devices, voice recognition devices, electronic pen devices, and mass storage devices such as tape drives or digital video disks ("DVDs").

The paragraph at page 5, lines 13-30, is amended as follows:

The peripheral devices usually communicate with the processor over one or more peripheral component interconnect ("PCI") **[slot]** **slots** 166, universal serial bus ("USB") ports 175, or integrated device electronics ("IDE") connectors 176. PCI card slots 166 may use card/bus controller 165 to connect to one or more buses such as host bus 120, PCI bus 160, and low pin count ("LPC") bus 180, with the buses communicating with each other through the use of one or more hubs such as graphics controller memory hub 140 and I/O controller hub 170. Typical systems such as example computer system 100 often include network interface **[cabling]** **card** slots 198 to accommodate network cards that mediate between the computer and the physical media over which transmissions to and from computer system 100 travel. USB ports 175 and IDE connectors 176 may connect to one or more of hubs 140, 170. The hubs may communicate with each other through the use of one or more links such as hub link 190. Generally, I/O devices can also be accommodated by parallel port 193 and serial ports 194 that are coupled to I/O controller 187 that is in turn coupled to LPC bus 180. Typical computer systems often include monitor 168 coupled to a display controller 131 coupled to graphics memory controller hub 140 by a graphics bus 135 and main memory 150 coupled to graphics memory controller hub 140 by a system management ("SM") bus 130. Finally, a typical computer system also includes software modules known as the basic input/output system (BIOS) (not shown). The BIOS code is either copied from an external medium such as a CD to, or stored on, memory area 200 in firmware hub 186.

The paragraph at page 6, line 24, through page 7, line 3, is amended as follows:

From interface cable 210, the signals from the red, green, and blue output gates, 196A, 196B, and 196C, respectively, travel to video amplifiers 169, [respectively,] and control the illumination of red, green, and blue phosphor dots on the screen of monitor 168. The signals for the horizontal and vertical synchronization output gates 197A and 197B travel from interface cable 210 to horizontal and vertical synchronization receiver input gates 171A and 171B, respectively, (together, receiver input gates 171) in monitor 168, from receiver input gates 171 to horizontal and vertical synchronization processors 172A and 172B, respectively, (together, synchronization or sync processor 172), and from sync processor 172 to horizontal and vertical deflectors 173A and 173B, respectively, which control the deflection of the electron beam used to illuminate the screen of monitor 168.

The paragraph at page 8, lines 12-17, is amended as follows:

During the period from time t_o to time t_1, h-sync output gate 197A "sees" h-sync line 211A to be terminated with the effective impedance Z_c of the interface line, output voltage V_O of h-sync output gate 197A rises from $V_O = 0$. During the period from time t_1 to time t_2 output voltage V_O substantially levels off at the voltage level appropriate to drive a load of impedance Z_C. This substantial leveling-off is called a "pedestal" in the output signal of h-sync output gate 197A. In Figure 4, this pedestal voltage level is designated as [V_{P1}] V_{p1}.

The paragraph at page 8, line 26-29, is amended as follows:

During the period from time t_3 to time t_4, the output voltage of h-sync output gate 197A substantially levels off again, forming another pedestal, because h-sync line 211A once again appears to h-sync output gate 197A to be terminated with the effective impedance Z_C of the interface line. This pedestal has voltage [V_{P2}] V_{p2}.